Commissioning of the SPADIC 1.0 Amplifier / Digitizer Chip*

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The SPADIC chip has been developed for the readout of the CBM TRD. The latest version SPADIC 1.0 has 32 channels on an area of $5 \times 5\,\mathrm{mm}^2$. The chip is fully functional and has been extensively tested in 2013.

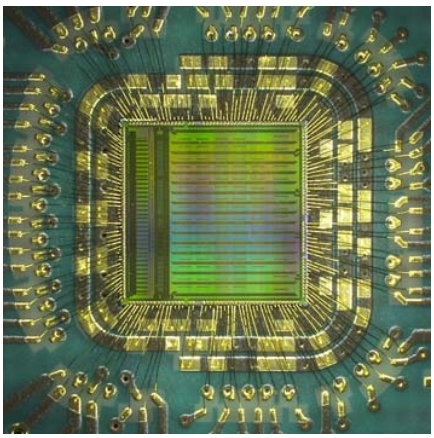

Figure 1: SPADIC1.0 chip bonded to readout PCB.

Chip Description

SPADIC 1.0 contains 32 identical channels on a die of $5 \times 5\,\mathrm{mm}^2$ size. It is fabricated in the 180 nm technology from UMC. The digital part uses custom made mixed mode standard cells and 44 SRAM blocks for data buffering. Each channel contains

- A charge amplifier / first order shaper ($\tau = 80\,\mathrm{ns}$) for positive input pulses with a noise of $\approx 800\,\mathrm{e}$ at $C_{in} = 30\,\mathrm{pF}$. This part consumes $\approx 5\,\mathrm{mW}$. In addition an experimental frontend for negative pulses is available.
- A $25\,\mathrm{MHz}$, $4.8\,\mathrm{mW}$ pipeline ADC with 9 bit output and an ENOB of > 8 Bit.
- A fully programmable digital IIR filter with 4 first order stages (16 bit processing, 6 bit coefficients).
- A sophisticated hit detection logic with differential threshold option for double hit detection and forced 'neighbor' trigger from channels on the same chip or even from different chips.
- A unit to pick an arbitrary set of amplitude samples from each pulse.
- A time ordered derandomization FIFO.
- Various error detection and recovery features (mainly for full buffers).

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The data link backend implements for the first time the CBMNet protocol on an ASIC. It sends out the agglomerated hit data in a compact data format over two serial LVDS links running at up to 500 Mbps. In order to simplify system design as much as possible, SPADIC 1.0 contains all further required infrastructure (current reference, bias DACs, monitoring busses, test pulse injectors) required to operate the chips with a minimum of external components and signals. For simplified assembly of detector readout modules, some chips have been packaged in QFP176 carriers of $26 \times 26\,\mathrm{mm}^2$ size.

Test Environment

The chip is bonded to an adapter board (Fig. 1) which is connected to a custom FPGA board holding a CBM net receiver firmware. The FPGA is accessed through USB2.0 using multi threaded Linux applications allowing for configuration of all chip settings, injections and data readout.

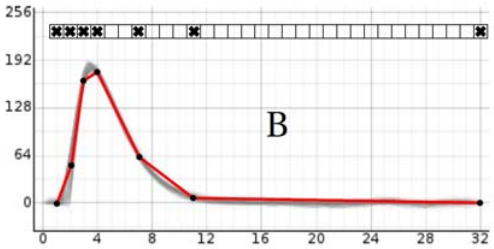

Figure 2: Samples sent out for a pulse using selection mask.

Results

All features of the chip have been operated successfully. Only few minor bugs have been identified which do not prevent chip operation on detectors. As just one example, Fig. 2 shows how interesting samples in one pulse can be picked using a freely programmable mask.

References

[1] M. Krieger, "Self-triggered charge pulse processing ASIC", Conference Proceedings of the TWEPP-13, Perugia, Italy, September 2013

[2] T. Armbruster, P. Fischer, M. Krieger and I. Peric, "Multi-Channel Charge Pulse Amplification, Digitization and Processing ASIC for Detector Applications", 2012 NSS Conference Record (IEEE), Anaheim, USA, October 2012

[3] http://spadic.uni-hd.de/

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